REMARKS/ARGUMENTS

Prior to this Reply to Office Action, Claim 1 was pending in the present application. Through this Reply, Claim 1 has been amended. Accordingly, following the entry of the present amendment, Claim 1 will be pending in the present application. Support for this amendment is found, at least, at page 22, line 20 to page 23, line 3 of the present specification. Accordingly, no new matter has been added. Applicant respectfully requests reconsideration of the present application in view of the amendment and following remarks. Also, the amendment includes deleting the process limitations pointed out by the Examiner.

Claim Objections

In order to overcome the claim objections, Claim 1, line 1 is amended to "A thin film" and line 4 is amended to "the insulator substrate and the gate electrode".

§103(a) Obviousness Rejection of Claim 1

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai et al. in view of Ono et al. The present invention, as claimed in Claim 1, is directed to a bottom gate type TFT having a gate electrode having a "pair of tapered end portions with inclined surfaces, an angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of 10° to 40° so that a uniform grain size of the polycrystalline silicon film is acquired above the center portion and the pair of tapered end portions" (emphasis added). Defining an angle of each of the pair of tapered end portions within a range of 10° to 40° is preferable to secure a gate withstand voltage and prevent the inclined surfaces of the pair

not true

of tapered end portions from increasing. An angle smaller than 10° causes the disadvantages recited at page 22, line 30 to page 23, line 3 of the present specification and makes it difficult to control a gate line width of TFT. It is important to control the gate line width, as gate lines within a screen of LCD are very fine. Increase of the variation in the gate line width results in a poor display. Furthermore, there are disadvantages associated with the apparatus which is required to form gate lines with high precision, in which the processing time of forming the gate lines becomes relatively long. An angle greater 40° causes the disadvantages recited at page 22, lines 27-29 of the present specification. Furthermore, if a relatively thick gate insulating film is formed on a gate electrode, a space is formed between a tip portion of each tapered end portion and the thick gate insulating film, which lowers the gate withstand voltage.

Tsai et al. (U.S. Patent No. 5,892,246) is directed to a polysicilicon TFT formed by a laser annealing step to cause an amorphous silicon layer to crystallize into polysilicon. However, Tsai et al. does not disclose that a gate electrode includes a pair of tapered end portions each having an angle within a range of 10° to 40° so that a uniform grain size of the polychrystalline silicon film is acquired above the centered portion and the pair of tapered end portions.

Ono et al. (U.S. Patent No. 5,760,854) is directed to a liquid crystal display apparatus including a gate electrode (2) having an end portion shaped in a taper of 6° to 10° in order to decrease the probability of causing cracks at the overriding portion of a gate insulating layer (4) which comprises a silicon nitride film (column 18, lines 7-11). However, Ono et al. does not teach or suggest setting the taper angle of the end portion within 10° to 40° in order to acquire a uniform grain size of the polycrystalline silicon film above the center portion and the pair of tapered end portions.

Accordingly, Applicant submits the present is not obvious by the combination of Tsai et al. and Ono et al.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version With Markings to Show Changes Made**."

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Twice Amended) [thing] A thin film transistor comprising:

an insulator substrate;

a gate electrode located on the insulator substrate;

a gate insulator film provided above the insulator substrate [an] and the gate electrode; and

a polycrystalline silicon film located on the gate insulator film, [the polycrystalline silicon film being formed by irradiating a laser beam on a surface of an amorphous silicon film to heat the amorphous silicon film,]

the gate electrode having a center portion with a flat surface and a pair of tapered end portions with inclined surfaces, an angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of [5°] 10° to 40° so that a uniform grain size of the polycrystalline silicon film is acquired above the center portion and the pair of tapered end portions, a gate withstand voltage of the thin film transistor is secured, and the inclined surfaces of the pair of tapered end portions are prevented from increasing [, wherein the laser beam is scanned on the surface of the amorphous silicon film such that a first portion of the amorphous silicon film above the gate electrode receives greater crystallization laser energy than a second portion of the amorphous silicon film above the insulator substrate, and a third portion of the amorphous silicon film above the center portion receives greater crystallization laser energy than fourth portions of the amorphous silicon film above tapered end portions].